What is claimed is:

1. A memory device controller comprising:

an updateable register bank adapted to send a first signal to an analog/memory core of the memory device for controlling operation of the analog/memory core, the analog/memory core comprising an array of flash memory cells and supporting analog access circuitry;

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and to send a third signal to the register bank for updating the register bank;

a select register coupled to the register bank; and

a first processor coupled to the bus controller and the select register.

2. The memory device controller of claim 1, further comprising an expression checker coupled between the first processor and the bus controller.

3. The memory device controller of claim 1, further comprising a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase.

4. The memory device controller of claim 1, further comprising a clock for sending clock signals to at least one of the first processor, the register bank, and the select register.

5. The memory device controller of claim 4, wherein the clock comprises four clock phases.

6. The memory device controller of claim 1, further comprising a controller interface coupled to the first processor and couplable to at least one of a command user interface of the memory device and a second processor located externally of the memory device.

7. The memory device controller of claim 6, wherein the controller interface comprises a suspension controller for causing a suspend command received thereat to be sent to the first processor at a pre-selected time of an operating cycle of the memory device controller.

8. The memory device controller of claim 1, wherein the first signal comprises an address of the analog/memory core.

9. The memory device controller of claim 1, wherein the bus controller comprises an arithmetic logic unit adapted to perform at least one arithmetic operation on at least one of the second signal and data received from the first processor.

10. The memory device controller of claim 1, wherein the first processor comprises a storage device that contains one or more algorithms that include instructions for controlling operation of the memory device controller.

11. A memory device controller comprising:

an updateable register bank adapted to send a first signal to an analog/memory core of the memory device for controlling operation of the analog/memory core;

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank;

a select register coupled to the register bank;

a first processor coupled to the bus controller and the select register;

an expression checker coupled between the first processor and the bus controller;

a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase; and

a controller interface coupled to the first processor and couplable to at least one of a command user interface of the memory device and a second processor located externally of the memory device.

12. The memory device controller of claim 11, wherein the bus controller comprises an arithmetic logic unit adapted to perform at least one arithmetic operation on at least one of the second signal and data received from the first processor.

13. The memory device controller of claim 11, wherein the controller interface comprises a suspension controller for causing a suspend command received thereat to be sent to the first processor at a pre-selected time of an operating cycle of the first controller.

14. A memory device comprising

an analog/memory core comprising an array of flash memory cells and supporting analog access circuitry;

a memory device controller comprising:

an updateable register bank adapted to send a first signal to the analog/memory core for controlling operation of the analog/memory core;

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank;

a select register coupled to the register bank; and

a first processor coupled to the bus controller and the select register; and

a command user interface coupled to the first controller and couplable to a second processor located externally of the memory device.

15. The memory device of claim 14, wherein the memory device controller further comprises an expression checker coupled between the first processor and the bus controller.

16. The memory device of claim 14, wherein the bus controller comprises an arithmetic logic unit adapted to perform at least one arithmetic operation on at least one of the second signal and data received from the first processor.

17. The memory device of claim 14, wherein the memory device controller further comprises a suspension controller for causing a suspend command received thereat to be sent to the first processor at a pre-selected time of an operating cycle of the memory device controller.

18. A memory device comprising

an analog/memory core comprising an array of flash memory cells and supporting analog access circuitry;

a memory device controller comprising:

an updateable register bank adapted to send a first signal to the analog/memory core for controlling operation of the analog/memory core;

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank;

a select register coupled to the register bank; and

a first processor coupled to the bus controller and the select register;

an expression checker coupled between the first processor and the bus controller; and

a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase; and

a command user interface coupled to the memory device controller and couplable to a second processor located externally of the memory device.

19. A memory system comprising:

a first processor; and

a memory device comprising:

an analog/memory core comprising an array of flash memory cells and supporting analog access circuitry;

a memory device controller coupled to the first processor, the memory device controller comprising:

an updateable register bank adapted to send a first signal to the analog/memory core for controlling operation of the analog/memory core;

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank;

a select register coupled to the register bank; and

a second processor coupled to the bus controller and the select register; and

a command user interface coupled to the memory device controller and to the first processor.

20. The memory system of claim 19, wherein the memory device controller further comprises an expression checker coupled between the second processor and the bus controller.

21. The memory system of claim 19, wherein the bus controller comprises an arithmetic logic unit adapted to perform at least one arithmetic operation on at least one of the second signal and data received from the second processor.

22. The memory system of claim 19, wherein the memory device controller further comprises a suspension controller for causing a suspend command received from the first processor to be sent to the second processor at a pre-selected time of an operating cycle of the memory device controller.

23. The memory system of claim 19, wherein the memory device controller further comprises a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase.

24. A method of operating a memory device controller, the method comprising:

receiving first data at a bus controller of the memory device controller from a first register of a register bank of the memory device controller;

sending second data from the bus controller to the first or a second register of the register bank for updating the register bank; and

sending a control signal from a third register of the register bank to an analog/memory core of the memory device for controlling operation of the analog/memory core, the analog/memory core comprising an array of flash memory cells and supporting analog access circuitry.

25. The method of claim 24, further comprising processing the first data at the bus controller to produce the second data.

26. The method of claim 25, wherein processing the first data at the bus controller is in response to receiving a signal from a processor of the memory device controller.

27. The method of claim 25, wherein processing the first data at the bus controller comprises processing the first data in combination with third data received at the bus controller from a processor of the memory device controller.

28. The method of claim 24, wherein sending second data from the bus controller to the first or the second register comprises:

sending the second data to a transfer register during a first clock phase;

holding the second data at the transfer register until a second clock phase; and

sending the second data to the first or the second register during the second clock phase.

30. The method of claim 24, further comprising receiving an input signal at a third register of the register bank from the analog/memory core, the third signal indicative of operation of the analog/memory core.

31. The method of claim 24, further comprising receiving a control signal at a select register of the memory device controller from a processor of the memory device controller before receiving the first data at the bus controller for selecting the first register.

32. A method of operating a memory device controller, the method comprising:

decrementing a number at a bus controller of the memory device controller when the number is not at a predetermined value;

going to a next address of an algorithm of the memory device controller when the number is not the predetermined value;

jumping over one or more addresses of the algorithm when the number is at the predetermined value; and

sending the number to a register bank of the memory device controller.

33. The method of claim 32, further comprising receiving the number at the bus controller from the register bank before decrementing the first number.

34. The method of claim 32, further comprising, before decrementing the number:

receiving the number at the bus controller from a processor of the memory device controller; and

sending the number to the register bank.

35. The method of claim 32, further comprising checking the number at an expression checker of the memory device controller after decrementing the number to determine whether the number is at the predetermined value.

36. The method of claim 32, further comprising receiving a control signal at the bus controller from a processor of the memory device controller that causes the bus controller to decrement the number.

37. The method of claim 32, further comprising sending a control signal from the register bank to an analog/memory core of the memory device before sending the number to the register bank.

38. A method of operating a controller for a memory device, the method comprising:

receiving a first command at a first latch of the controller from a first processor external to the memory device;

sending the first command to a second latch of the controller upon receiving a second command at the first latch from a command user interface of the memory device;

sending the first command to a first gate of the controller during a first clock phase of the controller;

sending the first command to a second gate of the controller upon receiving a control signal at the first gate from a second processor of the controller, wherein the second processor generates the control signal in response to the second processor executing an instruction of an algorithm of the second processor;

sending the first command to a third latch of the controller during a second clock phase of the controller;

sending the first command to the second processor; and

resetting the third latch.

39. The method of claim 38, further comprising suspending execution of the algorithm of the second processor upon receiving the first command at the second processor.

40. The method of claim 38, further comprising resetting the first and second latches when resetting the third latch.